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1 Supporting sequential assumptions in hybrid verification

Ed Cerny, Ashvin Dsouza, Kevin Harer, Pei-Hsin Ho, Tony Ma

January 2005 **ASP-DAC '05:** Proceedings of the 2005 Asia and South Pacifi

Publisher: ACM

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We present a method for using a set of temporal properties (SVA, PSL, for industrial-strength hybrid verification that combines formal methods demonstrate the effectiveness ...

2 A framework for object oriented hardware specification, verification, a

T. Kuhn, T. Oppold, M. Winterholer, W. Rosenstiel, Marc Edwards, Yaron K

June 2001 **DAC '01:** Proceedings of the 38th annual Design Automation

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We describe two things. First, we present a uniform framework for obje hardware. For this purpose the object oriented language "e" is introduce environment that ...

Keywords: high-level synthesis, object oriented hardware modeling, ve

3 Modelling hardware verification concerns specified in the e language

Darren Galpin, Cormac Driver, Siobhán Clarke

March 2009 **AOSD '09:** Proceedings of the 8th ACM international conferen development

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e is an aspect-oriented hardware verification language that is widely us through the development and execution of testbenches. In recent years developed at ...

Keywords: aspect-oriented modelling, e, hardware verification, theme,

4 Object oriented hardware synthesis and verification

T. Kuhn, T. Oppold, C. Schulz-Key, M. Winterholer, W. Rosenstiel, M. Edwa
September 2001 **ISSS '01:** Proceedings of the 14th international symposiur
Publisher: ACM
Full text available: Pdf (96.62 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 11, Downloa

The synthesis of hardware from object oriented specifications is present that has been proven to be highly efficient for the verification of hardwa

Keywords: high-level synthesis, object oriented hardware modeling, ve

5 Common Reusable Verification Environment for BCA and RTL Mode

Giuseppe Falconeri, Walid Naifer, Nizar Romdhane
March 2005 **DATE '05: Proceedings of the conference on Design, Aut 3** , Volume 3
Publisher: IEEE Computer Society
Full text available: Pdf (142.01 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 11, Downloa

This paper deals with a common verification methodology and environm aim is to save effort by avoiding the same work done twice by different for the two design views. Applying ...

6 Random stimulus generation using entropy and XOR constraints

Stephen M. Plaza, Igor L. Markov, Valeria Bertacco
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Publisher: ACM
Full text available: Pdf (1.96 MB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 41, Downloa

Despite the growing research effort in formal verification, constraint-ba part of design validation, especially for large design components where stimulating important ...

7 A comparison of three verification techniques: directed testing, pseu checking

Mike G. Bartley, Darren Galpin, Tim Blackmore
June 2002 **DAC '02:** Proceedings of the 39th annual Design Automation
Publisher: ACM Request Permissions
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This paper describes the verification of two versions of a bridge betwee performed just as the Infineon Technologies Design Centre in Bristol wa Specman) and property ...

8

Design experience of a chip multiprocessor merlot and expeciation l
Satoshi Matsushita
October 2002 **ISSS '02:** Proceedings of the 15th international symposium c
Publisher: ACM
Full text available: Pdf (797.44 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 21, Downloa

We have fabricated a Chip Multiprocessor prototype code-named Merlot multithreading architecture. On Merlot, multiple threads provide wider i level parallel (ILP) processors like superscalar ...

Keywords: CMP, chip multiprocessor, deign experience, functional veri

9 Shortening the verification cycle with synthesizable abstract models
Alon Gluska, Lior Libis
July 2009 **DAC '09:** Proceedings of the 46th Annual Design Automation
Publisher: ACM Request Permissions
Full text available: Pdf (119.79 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 12, Downloads (12 Months): 12, Downlo

Abstract modeling has been widely used, albeit independently, for both of SoC designs. In this paper we show that proper selection of modeling the same code useful for ...

Keywords: abstract modeling, logic design, verification

10 Specification-driven directed test generation for validation of pipeline
Prabhat Mishra, Nikil Dutt
July 2008 **Transactions on Design Automation of Electronic Syster**
Publisher: ACM Request Permissions
Full text available: Pdf (533.05 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 12, Downloads (12 Months): 69, Downlo

Functional validation is a major bottleneck in pipelined processor design design complexity and lack of efficient techniques for directed test gene overall validation effort, ...

Keywords: Model checking, functional validation, test generation

11 Functional Coverage Driven Test Generation for Validation of Pipelir
Prabhat Mishra, Nikil Dutt
March 2005 **DATE '05: Proceedings of the conference on Design, Aut 2** , Volume 2
Publisher: IEEE Computer Society
Full text available: Pdf (144.35 KB) Additional Information: full citation, abstr

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Functional verification of microprocessors is one of the most complex ar on-chip design process. A significant bottleneck in the validation of such coverage metric. This ...

12 Property-Specific Testbench Generation for Guided Simulation
Aarti Gupta, Albert E. Casavant, Pranav Ashar, Akira Mukaiyama, Kazutosh
January 2002 **ASP-DAC '02:** Proceedings of the 2002 Asia and South Pacifi
Publisher: IEEE Computer Society
Full text available: Publisher Site , Pdf (208.21 KB) Additional Information: full citatio

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 18, Downloa

Simulation continues to be the primary technique for functional validatic simulation vectors be effective in targeting the types of bugs designers coverage metrics. The overall ...

Keywords: guided simulation, intelligent testbench generation, witness symbolic model checking, approximate model checking, iterative refiner

13 Scheduling-based test-case generation for verification of multimedia
Amir Nahir, Avi Ziv, Roy Emek, Tal Keidar, Nir Ronen
July 2006 **DAC '06:** Proceedings of the 43rd annual Design Automation
Publisher: ACM Request Permissions
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Multimedia SoCs are characterized by a main controller that directs the charge of a stage in the processing of a media stream. The verification to time-to-market ...

Keywords: functional verification, system on a chip, test generation

14 Coverage-oriented verification of banias
Alon Gluska
June 2003 **DAC '03:** Proceedings of the 40th annual Design Automation
Publisher: ACM Request Permissions
Full text available: Pdf (178.40 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 17, Downloa

The growing complexity of state-of-art microprocessors dictates the use Functional coverage was widely applied in the verification of Banias, Int solely for the mobile computing ...

Keywords: coverage, functional coverage, logic design, logic verificatic

15 Verification of chip multiprocessor memory systems using a relaxed
Ofer Shacham, Megan Wachs, Alex Solomatnikov, Amin Firoozshahian, Ste
November 2008 **MICRO '08:** Proceedings of the 2008 41st IEEE/ACM Interr
Publisher: IEEE Computer Society

Full text available: Pdf (643.10 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 66, Downlo

Verification of chip multiprocessor memory systems remains challengin validate protocols, simulation is still the dominant method used to valid Having a memory scoreboard, a high-level ...

16 A mixed-signal verification kit for verification of analogue-digital circu
G. Bonfini, M. Chiavacci, R. Mariani, E. Pescari
March 2006 **DATE '06:** Proceedings of the conference on Design, automat
Publisher: European Design and Automation Association
Full text available: Pdf (202.50 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 8, Download

This paper presents an innovative approach for analogue and mixed-sig kit" that makes use of concepts used in state-of-art digital verification, coverage elaboration, ...

17 StressTest: an automatic approach to test generation via activity mo
Ilya Wagner, Valeria Bertacco, Todd Austin
June 2005 **DAC '05:** Proceedings of the 42nd annual Design Automation
Publisher: ACM Request Permissions
Full text available: Pdf (896.33 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 32, Downloa

The challenge of verifying a modern microprocessor design is an overwh architectures combined with heavy time-to-market pressure have force immense verification teams in the hope ...

Keywords: architectural simulation, directed-random simulation, high-

18 Depth-driven verification of simultaneous interfaces
Ilya Wagner, Valeria Bertacco, Todd Austin
January 2006 **ASP-DAC '06:** Proceedings of the 2006 Asia and South Pacifi
Publisher: IEEE Press
Full text available: Pdf (234.57 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 6, Download

The verification of modern computing systems has grown to dominate t success as designs continue to be released with latent bugs. This trend integrated system-on-a-chip ...

19 New methods and coverage metrics for functional verification
Vasco Jerinić, Jan Langer, Ulrich Heinkel, Dietmar Müller
March 2006 **DATE '06:** Proceedings of the conference on Design, automat
Publisher: European Design and Automation Association
Full text available: Pdf (174.19 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 20, Downloa

An ever increasing portion of design effort is spent on functional verifica possible combinations of a design's attributes is likely to be very large r this space. State-of-the-art ...

20 FSM-based transaction-level functional coverage for interface compl
Man-Yun Su, Che-Hua Shih, Juinn-Dar Huang, Jing-Yang Jou
January 2006 **ASP-DAC '06:** Proceedings of the 2006 Asia and South Pacifi
Publisher: IEEE Press
Full text available: Pdf (285.81 KB) Additional Information: full citation, abstr

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 27, Downloa

Interface compliance verification plays a very important role in modern quantitative analysis of simulation completeness, adequate coverage m propose a finite state machine (FSM) ...